

## EAST Search History

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
S17 2	0	(714/746.ccls.) and ((logic adj circuit\$1) and (ECC or (error adj control adj code))) and memory and transparent and (transient adj disturbance))	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2007/05/09 17:44
S17 3	0	(714/55.ccls.) and ((logic adj circuit\$1) and (ECC or (error adj control adj code))) and memory and transparent and (transient adj disturbance))	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2007/05/09 17:33
S17 4	0	(714/48.ccls.) and ((logic adj circuit\$1) and (ECC or (error adj control adj code))) and memory and transparent and (transient adj disturbance))	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2007/05/09 17:33
S17 5	0	(714/43.ccls.) and ((logic adj circuit\$1) and (ECC or (error adj control adj code))) and memory and transparent and (transient adj disturbance))	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2007/05/09 17:34
S17 6	0	(714/731.ccls.) and ((logic adj circuit\$1) and (ECC or (error adj control adj code))) and memory and transparent and (transient adj disturbance))	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2007/05/09 17:34
S17 7	0	(714/700.ccls.) and ((logic adj circuit\$1) and (ECC or (error adj control adj code))) and memory and transparent and (transient adj disturbance))	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2007/05/09 17:34
S17 8	0	(714/814.ccls.) and ((logic adj circuit\$1) and (ECC or (error adj control adj code))) and memory and transparent and (transient adj disturbance))	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2007/05/09 17:34
S17 9	0	(714/815.ccls.) and ((logic adj circuit\$1) and (ECC or (error adj control adj code))) and memory and transparent and (transient adj disturbance))	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2007/05/09 17:35

## EAST Search History

S18 0	0	(714/819.ccls.) and ((logic adj circuit\$1) and (ECC or (error adj control adj code)) and memory and transparent and (transient adj disturbance))	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2007/05/09 17:35
S18 1	0	(714/744.ccls.) and ((logic adj circuit\$1) and (ECC or (error adj control adj code)) and memory and transparent and (transient adj disturbance))	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2007/05/09 17:35
S18 2	0	(713/401.ccls.) and ((logic adj circuit\$1) and (ECC or (error adj control adj code)) and memory and transparent and (transient adj disturbance))	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2007/05/09 17:35
S18 3	0	(713/500.ccls.) and ((logic adj circuit\$1) and (ECC or (error adj control adj code)) and memory and transparent and (transient adj disturbance))	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2007/05/09 17:36
S18 4	0	(713/600.ccls.) and ((logic adj circuit\$1) and (ECC or (error adj control adj code)) and memory and transparent and (transient adj disturbance))	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2007/05/09 17:36
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S18 7	0	(714/48.ccls.) and ((logic adj circuit\$1) and memory and transparent and (transient adj disturbance))	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2007/05/09 17:34

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S18 8	0	(714/43.ccls.) and ((logic adj circuit\$1) and memory and transparent and (transient adj disturbance))	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2007/05/09 17:34
S18 9	0	(714/731.ccls.) and ((logic adj circuit\$1) and memory and transparent and (transient adj disturbance))	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2007/05/09 17:34
S19 0	0	(714/700.ccls.) and ((logic adj circuit\$1) and memory and transparent and (transient adj disturbance))	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2007/05/09 17:34
S19 1	0	(714/814.ccls.) and ((logic adj circuit\$1) and memory and transparent and (transient adj disturbance))	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2007/05/09 17:34
S19 2	0	(714/815.ccls.) and ((logic adj circuit\$1) and memory and transparent and (transient adj disturbance))	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2007/05/09 17:35
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S19 4	0	(714/744.ccls.) and ((logic adj circuit\$1) and memory and transparent and (transient adj disturbance))	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2007/05/09 17:35
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S19 6	0	(713/500.ccls.) and ((logic adj circuit\$1) and memory and transparent and (transient adj disturbance))	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2007/05/09 17:36
S19 7	0	(713/600.ccls.) and ((logic adj circuit\$1) and memory and transparent and (transient adj disturbance))	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2007/05/09 17:36
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S20 0	0	(714/48.ccls.) and ((logic adj circuit\$1) and (ECC or (error adj control adj code)) and memory and transparent and (transient adj disturbance\$1) and parity)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2007/05/09 17:40
S20 1	0	(714/43.ccls.) and ((logic adj circuit\$1) and (ECC or (error adj control adj code)) and memory and transparent and (transient adj disturbance\$1) and parity)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2007/05/09 17:40
S20 2	0	(714/731.ccls.) and ((logic adj circuit\$1) and (ECC or (error adj control adj code)) and memory and transparent and (transient adj disturbance\$1) and parity)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2007/05/09 17:40
S20 3	0	(714/700.ccls.) and ((logic adj circuit\$1) and (ECC or (error adj control adj code)) and memory and transparent and (transient adj disturbance\$1) and parity)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2007/05/09 17:40

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S20 4	0	(714/814.ccls.) and ((logic adj circuit\$1) and (ECC or (error adj control adj code))) and memory and transparent and (transient adj disturbance\$1) and parity)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2007/05/09 17:40
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S20 7	0	(714/744.ccls.) and ((logic adj circuit\$1) and (ECC or (error adj control adj code))) and memory and transparent and (transient adj disturbance\$1) and parity)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2007/05/09 17:41
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S21 2	0	(714/55.ccls.) and ((logic adj circuit\$1) and (ECC or (error adj control adj code)) and memory and transparent and (transient adj disturbance\$1))	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2007/05/09 17:45
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S21 5	0	(714/731.ccls.) and ((logic adj circuit\$1) and (ECC or (error adj control adj code)) and memory and transparent and (transient adj disturbance\$1))	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2007/05/09 17:46
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## EAST Search History

S22 0	0	(714/744.ccls.) and ((logic adj circuit\$1) and (ECC or (error adj control adj code)) and memory and transparent and (transient adj disturbance\$1))	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2007/05/09 17:47
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S22 3	0	(713/600.ccls.) and ((logic adj circuit\$1) and (ECC or (error adj control adj code)) and memory and transparent and (transient adj disturbance\$1))	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2007/05/09 17:47
S22 4	0	(714/746.ccls.) and ((logic adj circuit\$1) and memory and transparent and (transient adj disturbance\$1))	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2007/05/09 17:52
S22 5	0	(714/55.ccls.) and ((logic adj circuit\$1) and memory and transparent and (transient adj disturbance\$1))	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2007/05/09 17:49
S22 6	0	(714/48.ccls.) and ((logic adj circuit\$1) and memory and transparent and (transient adj disturbance\$1))	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2007/05/09 17:49
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## EAST Search History

S22 8	0	(714/731.ccls.) and ((logic adj circuit\$1) and memory and transparent and (transient adj disturbance\$1))	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2007/05/09 17:49
S22 9	0	(714/700.ccls.) and ((logic adj circuit\$1) and memory and transparent and (transient adj disturbance\$1))	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2007/05/09 17:49
S23 0	0	(714/814.ccls.) and ((logic adj circuit\$1) and memory and transparent and (transient adj disturbance\$1))	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2007/05/09 17:50
S23 1	0	(714/815.ccls.) and ((logic adj circuit\$1) and memory and transparent and (transient adj disturbance\$1))	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2007/05/09 17:50
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S23 3	0	(714/744.ccls.) and ((logic adj circuit\$1) and memory and transparent and (transient adj disturbance\$1))	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2007/05/09 17:50
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## EAST Search History

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## EAST Search History

S24 4	0	(714/815.ccls.) and ((logic adj circuit\$1) and memory and (transient adj disturbance\$1))	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2007/05/09 17:55
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S24 7	0	(713/401.ccls.) and ((logic adj circuit\$1) and memory and (transient adj disturbance\$1))	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2007/05/09 17:57
S24 8	0	(713/500.ccls.) and ((logic adj circuit\$1) and memory and (transient adj disturbance\$1))	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2007/05/09 17:58
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S25 2	26	nicolaidis-michael.IN.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2007/05/09 18:53
S25 7	8	((logic adj circuit\$1) and memory and transparent and (transient adj disturbance\$1))	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2007/05/09 19:02

## EAST Search History

S25 8	0	(714/758.ccls.) and ((logic adj circuit\$1) and memory and transparent and (transient adj disturbance\$1))	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2007/05/10 15:22
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S26 1	0	(714/799.ccls.) and ((logic adj circuit\$1) and memory and transparent and (transient adj disturbance\$1))	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2007/05/10 15:28

**EAST Search History**

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
S25 0	0	((logic adj circuit\$1) and (ECC or (error adj control adj code)) and memory and transparent and (transient adj disturbance\$1))	US-PGPUB	OR	OFF	2007/05/09 18:00
S25 1	4	((logic adj circuit\$1) and memory and transparent and (transient adj disturbance\$1))	US-PGPUB	OR	OFF	2007/05/09 19:01

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John Colter, Netscape Navigator

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